WHAT IS CLAIMED IS:

1. An current limiting circuit for a switch comprising:
    a. a switch connected to a power supply and a load;
    b. a shunt resistor having a first and second terminal, with the first terminal connected to the switch; and
    c. a control circuit connected to the second terminal of the resistor and to the load side of the switch;
    d. wherein the control circuit monitors the voltage across the switch and the voltage at the shunt resistor and limits the current through the switch when exceeding a current limit set by the shunt resistance as determined by the voltage at the shunt resistor and the voltage at the switch.

2. The circuit of claim 1 wherein the first terminal of the resistor is connected to the supply side of the switch.

3. The circuit of claim 1 wherein the first terminal of the resistor is connected to the load side of the switch.

4. The circuit of claim 1 wherein the switch is connected to the low side of the supply.

5. The circuit of claim 1 wherein the switch is connected to the high side of the supply.

6. The circuit of claim 5 further comprising a current source that sets a bias voltage drop across the shunt resistor and the current source is a linear temperature dependent source to compensate for variation of switch on resistance (RDS(on)) versus temperature.

7. The circuit of claim 1 wherein the switch is a N-channel FET transistor.

8. The circuit of claim 1 wherein the switch is a P-channel FET transistor.

9. The circuit of claim 1 wherein the circuit is incorporated in an integrated circuit except for the shunt resistor which is an external resistor.

10. The circuit of claim 3 wherein the circuit is incorporated in an integrated circuit except for the shunt resistor and an adjustment resistor connected to the current source, which are external resistors.

11. An current limiting circuit for a MOS transistor switch for a hot swap board application comprising:
    a. a switch connected to a power supply and a load;
    b. a shunt resistor having a first and second terminal, with the first terminal connected to the switch; and
    c. a control circuit connected to the second terminal of the resistor and to the load side of the switch;
    d. wherein the control circuit monitors the voltage across the switch and the voltage at the shunt resistor and limits the current through the switch when exceeding a current limit set by the shunt resistance.

12. The circuit of claim 11 wherein the first terminal of the resistor is connected to the supply side of the switch.

13. The circuit of claim 11 wherein the first terminal of the resistor is connected to the load side of the switch.

14. The circuit of claim 11 wherein the switch is connected to the low side of the supply.

15. The circuit of claim 11 wherein the switch is connected to the high side of the supply.

16. The circuit of claim 15 further comprising a current source that sets a bias voltage drop across the shunt resistor and the current source is a linear temperature dependent source to compensate for variation of switch on resistance (RDS(on)) versus temperature.

17. The circuit of claim 11 wherein the switch is a N-channel FET transistor.

18. The circuit of claim 11 wherein the switch is a P-channel FET transistor.

19. The circuit of claim 11 wherein the circuit is incorporated in an integrated circuit except for the shunt resistor which is an external resistor.

20. The circuit of claim 11 wherein the circuit is incorporated in an integrated circuit except for the shunt resistor and an adjustment resistor connected to the current source, which are external resistors.